

**Features**

- Frequency: 3.1GHz~3.5GHz
- Power Gain: 24dB
- Psat: 48dBm
- P.A.E.: 45%
- +28V@2.1A (quiescent peak current)
- Chip Size: 3.95mm×4.59mm×0.1mm

**Electrical Specification (TA=+25°C, Vg=-2.2V, Vd=+28V)**

Parameter	Min.	Typ.	Max.	Unit
Frequency	3.1~3.5			GHz
Psat		48		dBm
Power Gain		24		dB
Gain Flatness			±0.3	dB
P.A.E.		45		%
VSWRin			2.8	-
Operating Current			5.5	A

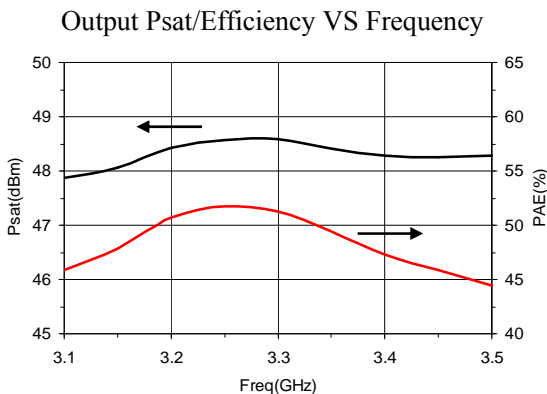
Note: 1) All chips have been on-chip 100% DC and RF tested.

2) Test Condition: Vd=+28V (1ms, 30% duty cycle); Vg=-2.2V, Pin=24dBm

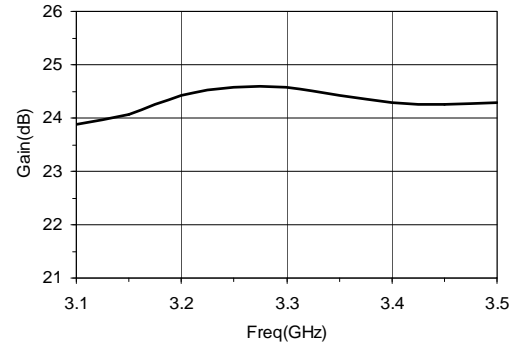
**Limited Rating Values**

Vds	+32V
Vgs	-5V
Input CW Power	+25dBm
Channel Temperature	+175°C
Storage Temperature	-65°C~+150°C

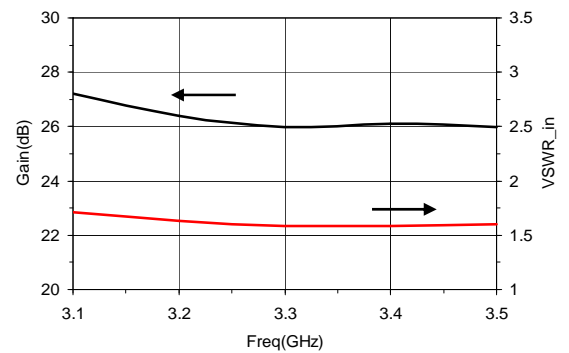
**Typical Testing Curves**



Power Gain VS Frequency

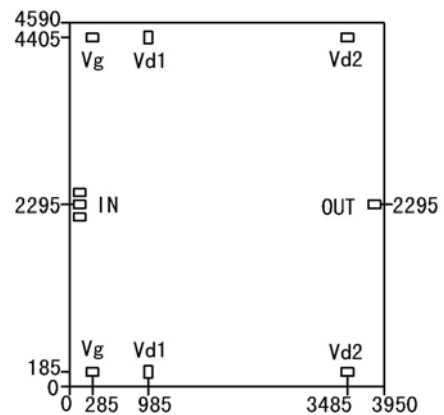


Linear Gain/VSWRin vs. Frequency



**Dimensions and Outline**

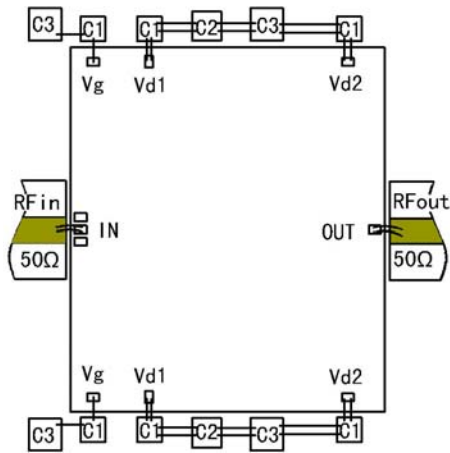
NC11624C-3135P64 outline



Note: The unit is um .

- Dimension of input/output pad: 150×100μm<sup>2</sup>,
- Dimension of bias pad Vg: 150×100μm<sup>2</sup>,
- Dimension of bias pad Vd1: 100×150μm<sup>2</sup>,
- Dimension of bias pad Vd1: 150×100μm<sup>2</sup>.

**Assembly Diagram**



Note: External capacitor C1=100pF, C2=1000pF,  
C3=10000pF.

**Attention**

- 1) Bonding with 80/20 Au/Sn. The temperature should be lower than 300°C and the time should be less than 30 seconds.
- 2) Gold wires (diameter: 25μm~30μm) are suggested to be used. The temperature of bonding platform should not exceed 250°C
- 3) Blocking capacitors in Input/Output are already integrated.
- 4) Antistatic protection should be taken.