

**Features**

- Frequency: 15GHz~17.5GHz
- Power Gain: 20dB
- Psat: 43dBm
- P.A.E.: 30%
- +28V @ 2.0A (Quiescent)
- Chip Size: 3.1mm×1.7mm×0.1mm

**Electrical Specification (TA=+25°C, Vd=+28V, Vg=-2.5V)**

Parameter	Min.	Typ.	Max.	Unit
Frequency	15~17			GHz
Power Gain	20	20.2	-	dB
Psat	43	43.2	-	dBm
P.A.E.	30	35	-	%
VSWRin	-	2.0	2.5	-
Dynamic Operating Current	3			A

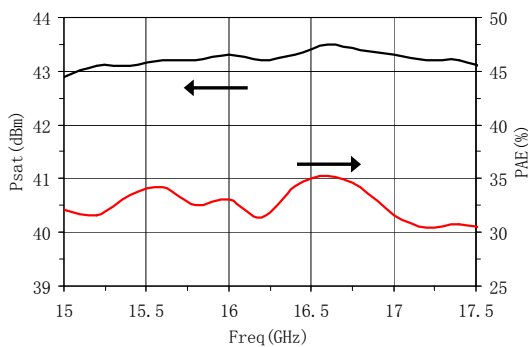
Note: 1) All chips have been on-chip 100% DC tested.  
 2) Test Condition: Vd=+28V, Vg=-2.5V, pulse width 100µs, duty cycle 10%, P<sub>in</sub>=22dBm.

**Limited Rating Values**

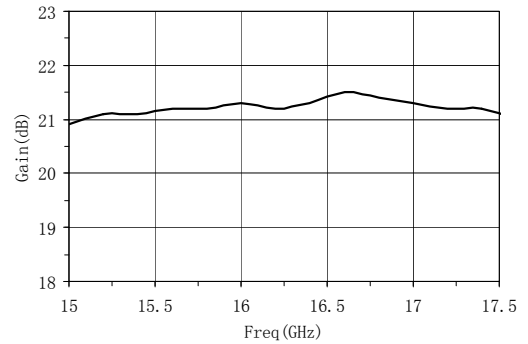
Max. Input Vd	+30V
Max. Input Power	+28dBm
Storage Temperature	-65°C ~ +150°C
Operating Temperature	-55°C ~ +125°C

**Typical Testing Curves**

Output Psat/Efficiency VS Frequency

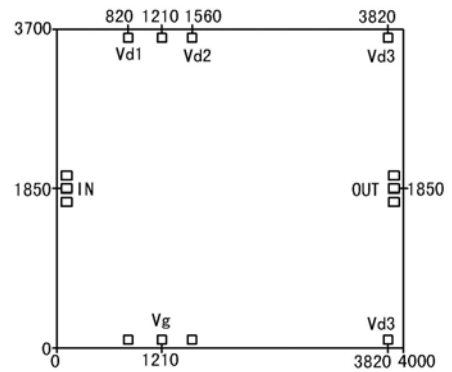


Power Gain VS Frequency



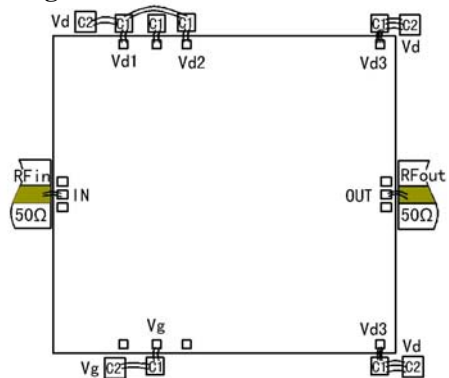
**Dimensions and Outline**

NC11615C-1517P20 outline



Note: The unit is um.  
 Dimension of input/output pad: 100×120µm<sup>2</sup>  
 Dimension of bias pad: 100×100µm<sup>2</sup>.

**Assembly Diagram**



Note : External capacitor c=100pF,c2=0.01µF. A 0.01µF capacitor should be added to the gate bias. Gold bonding wire diameter:25µm.

**Attention**

- 1) 2 bonding wires should be used for input/output. The length of the wires should be shorter than 350µm.
- 2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300°C and the time should be less than 30 seconds.
- 3) Blocking capacitors in Input/Output are already integrated.
- 4) Antistatic protection should be taken.