

**Features**

- Frequency: 16GHz~18GHz
- Power Gain: 20dB
- Psat: 45dBm
- P.A.E: 30%
- +28V @ 2.5A (quiescent state)
- Chip Size: 3.7mm×3.6mm×0.1mm

**Electrical Specification (TA=+25°C, Vd=+28V, Vg=-2.0V)**

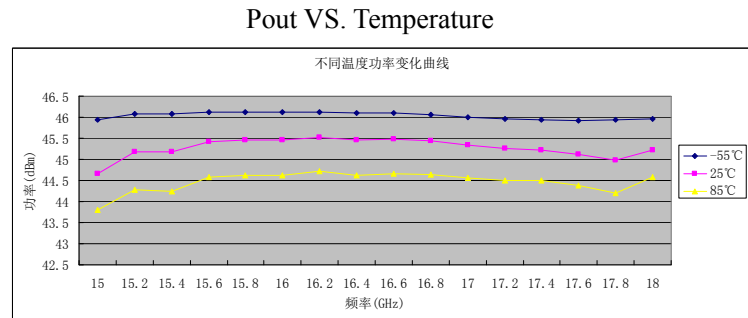
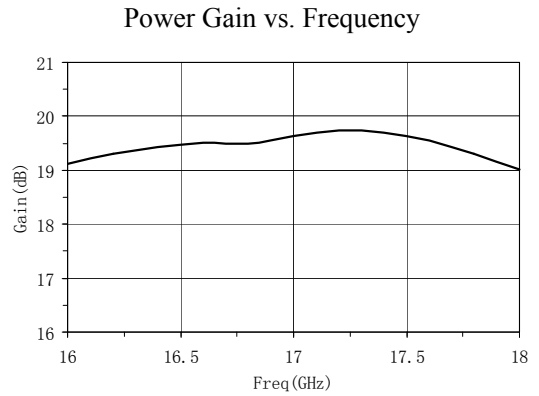
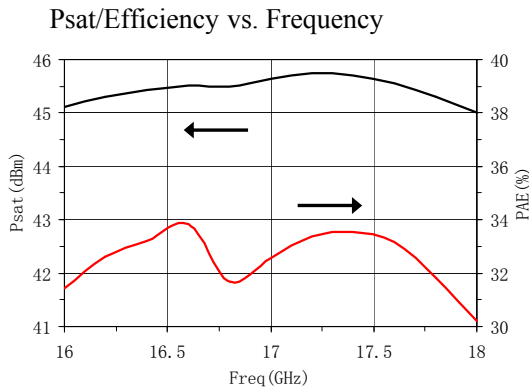
Parameter	Min	Typ.	Max	Unit
Frequency	16-18			GHz
Power Gain	19	20	—	dB
Saturation Pout	44.8	45.2	—	dBm
P.A.E	30	33	—	%
VSWRin	—	2.0	2.5	—
Dynamic Current	4			A

Note: 1) All chips have been 100% DC tested.  
 2) Test condition: Vd=+28V, Vg=-2.0V, pulse width 100μs, duty cycle 10%, P<sub>in</sub>=25dBm

**Limited Rating Values**

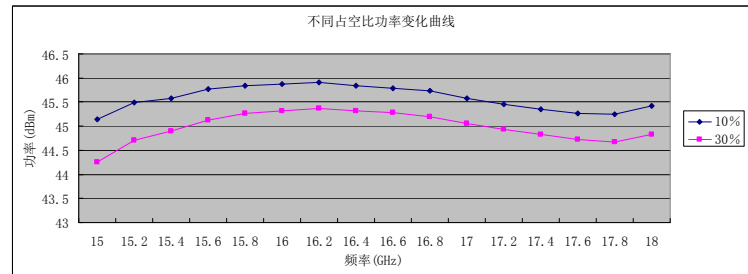
Max Input Vd	+30V
Max Input Power	+30dBm
Storage Temperature	-65°C ~ +150°C
Operation Temperature	-55°C ~ +85°C

**Typical Testing Curves**



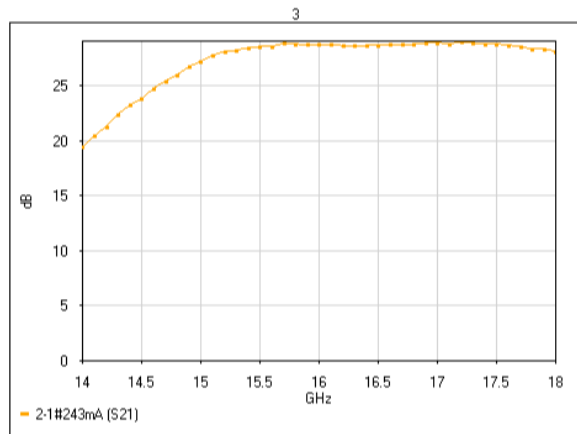
Power vs Frequency Curves under different temperature range  
 (V<sub>DS</sub>=28V, V<sub>GS</sub>=-2V, Duty Cycle 10%, Pulse width 100us)

**Power vs Frequency Curves under different Duty Cycle**

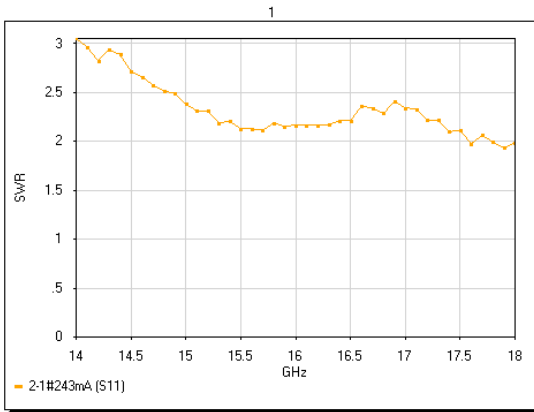


(V<sub>DS</sub>=28V, V<sub>GS</sub>=-1.8V)

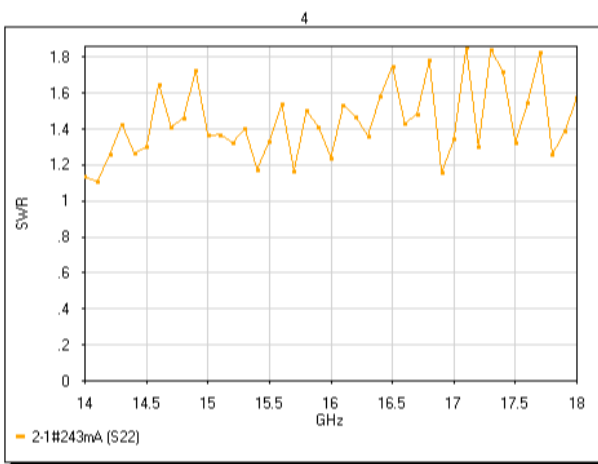
**Small Signal Testing Result:**



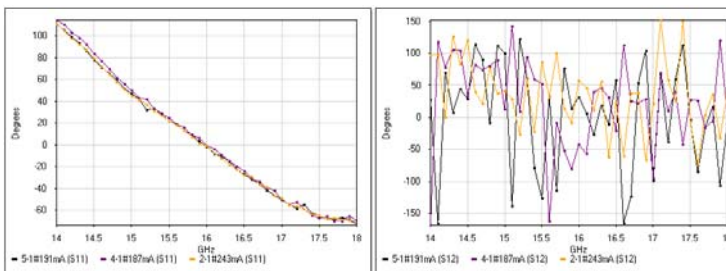
Small Signal Gain S21, (V<sub>DS</sub>=28V, V<sub>GS</sub>=-2V)



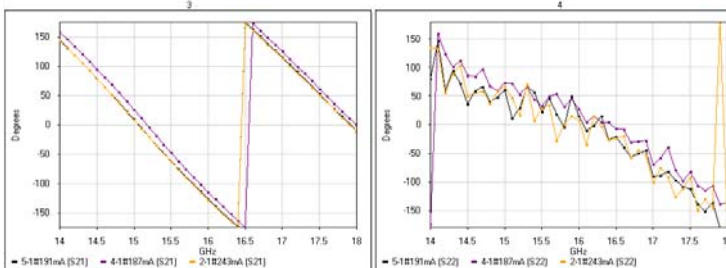
VSWRin, ( $V_{DS}=28V, V_{GS}=-2V$ )



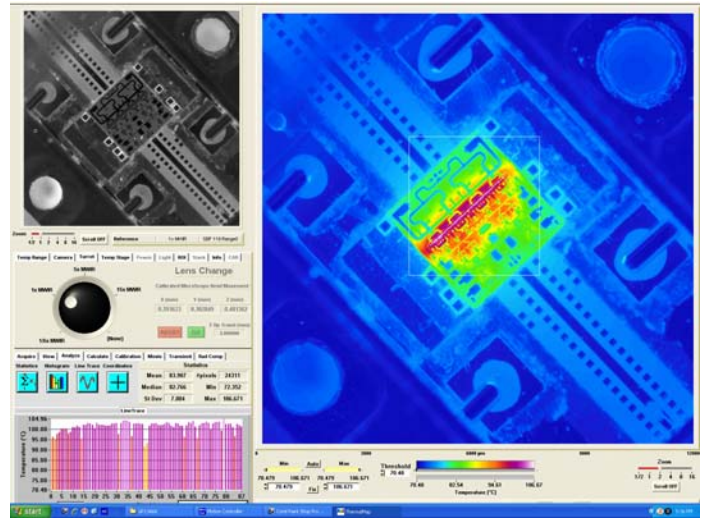
VSWRout, ( $V_{DS}=28V, V_{GS}=-2V$ )



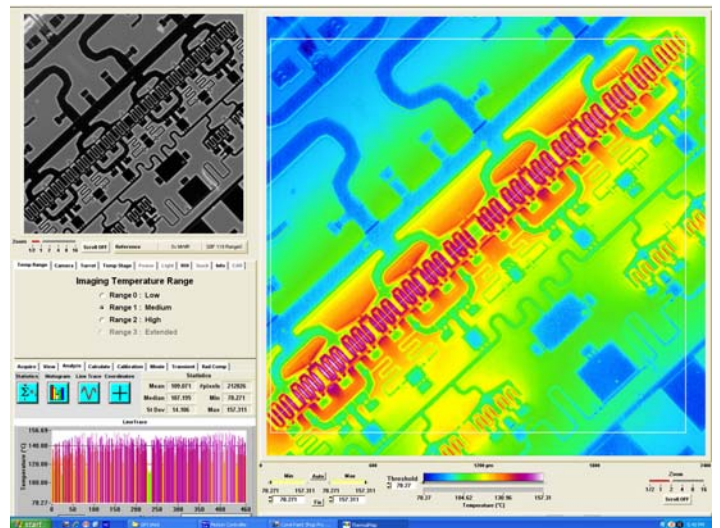
Phase Characteristics, ( $V_{DS}=28V, V_{GS}=-2V$ )



**Thermal Resistance Characteristics**



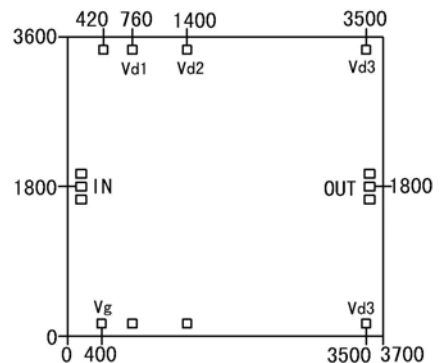
1X Pixel Thermal spread ( $V_{DS}=28V, I_{DS}=0.8A$ )



5X Pixel Thermal spread ( $V_{DS}=28V, I_{DS}=1.4A$ )

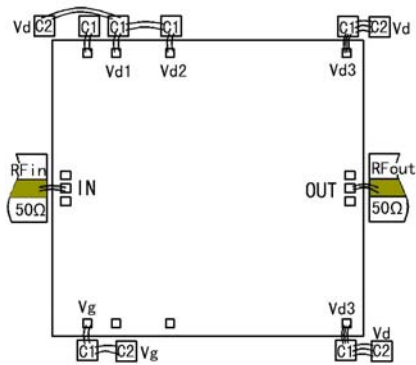
The thermal resistance is less than 3°C/W, and the power variation between high/low temperature is 1.5 dB, the power output will be dropped by 0.5 dB under 30% duty cycle.

**Dimension and Outline**



Note: The unit is  $\mu m$ . Input and output pad dimension:  $100 \times 120 \mu m^2$ . Bias pad dimension:  $100 \times 100 \mu m^2$

**Assembly Diagram**



Note: External capacitor  $c=100\text{pF}$ ,  $c_2=0.01\mu\text{F}$ . A  $0.01\mu\text{F}$  capacitor filter is needed for gate bias. Diameter of bonding gold wires:  $25\mu\text{m}$ .

**Attention:**

- 1) Two bonding wires are needed for input and output. The length should be shorter than  $350\mu\text{m}$ .
- 2) Bonding with 80/20 Au/Sn. The temperature should be lower than  $300\text{ }^\circ\text{C}$  and the time should be less than 30 seconds.
- 3) Blocking capacitors in Input/Output are already integrated.