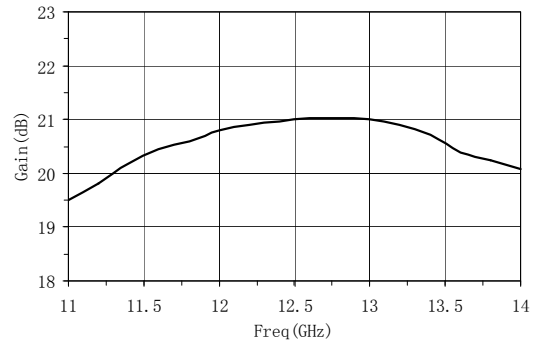


Features

- Frequency: 11GHz~14GHz
- Power Gain: 20dB
- Psat: 45.8dBm
- P.A.E.: 30%
- +28V @ 2.5A (Quiescent)
- Chip Size: 4.2mm×5.3mm×0.1mm

Power Gain VS Frequency

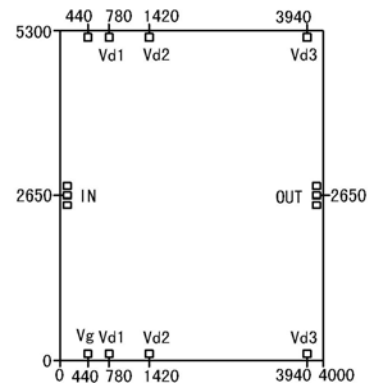


Electrical Specification (TA=+25°C, Vd=+28V, Vg=-2.5V)

Parameter	Min.	Typ.	Max.	Unit
Frequency	11-14			GHz
Power Gain		20		dB
Psat		45.8		dBm
P.A.E.		30		%
VSWRin		2.0	2.5	-
Dynamic Operating Current	4.5			A

Dimensions and Outline

NC11612C-1114P35 outline



- Note: 1) All chips have been on-chip 100% DC tested.
 2) Test Condition: Vd=+28V, Vg=-2.5V, pulse width 100μs, duty cycle 10%, P_{in}=25dBm.

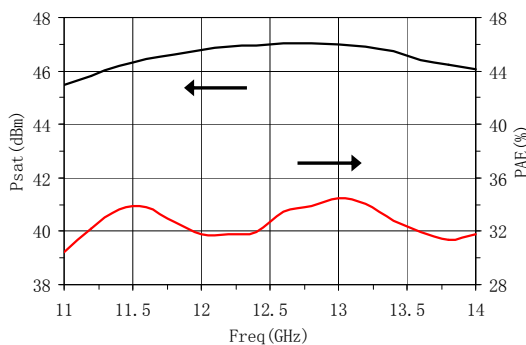
- Note: The unit is um.
 Dimension of input/output pad: 100×120μm².
 Dimension of bias pad :100×100μm².

Limited Rating Values

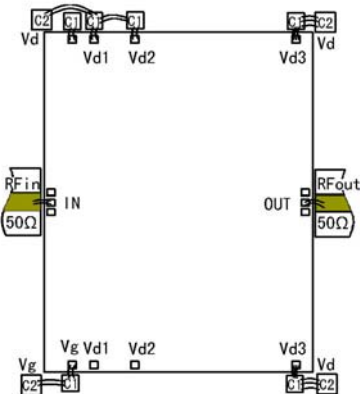
Max. Input Vd	+30V
Max. Input Power	+30dBm
Storage Temperature	-65°C ~ +150°C
Operating Temperature	-55°C ~ +85°C

Typical Testing Curves

Output Psat/Efficiency VS Frequency



Assembly Diagram



- Note : External capacitor c=100pF,c2=0.01μF. A 0.01μF capacitor should be added to the gate bias. Gold bonding wire diameter:25μm.

Attention

- 1) 2 bonding wires should be used for input/output. The length of the wires should be shorter than 350 μ m.
 - 2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300 $^{\circ}$ C and the time should be less than 30 seconds.
 - 3) Blocking capacitors in Input/Output are already integrated.
 - 4) Antistatic protection should be taken.
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