

**Features**

- Frequency: 0.9GHz~2.0GHz
- Power Gain: 25dB
- Psat: 43dBm
- P.A.E: 30%
- +26V@2.0A(quiescent state)
- Dimension: 3.14mm×5.14mm×0.10mm

**Electrical Specification** (TA=+25°C, Vg=-1.5V, Vd=+26V)

Parameter	Min.	Typ.	Max	Unit
Frequency	0.9-2.0			GHz
Psat		43.0		dBm
Power Gain		25		dB
Gain Flatness			±0.5	dB
P.A.E		33		%
VSWRin			2.0	-
Operating Current	2.8			A

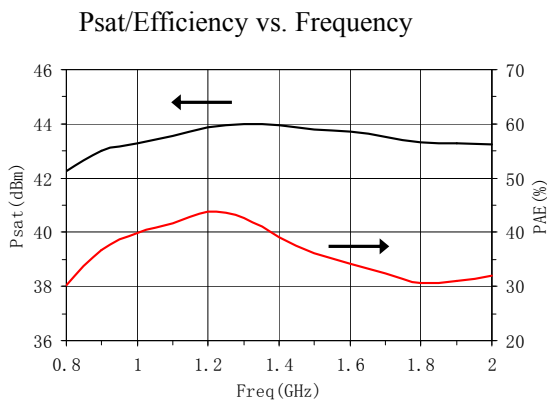
Note : 1) All chips have been 100% DC tested and RF tested.

2)Test Condition: Vd=+26V; Vg=-1.5V, pulse width 100μs, duty cycle 10%, P<sub>in</sub>=18dBm

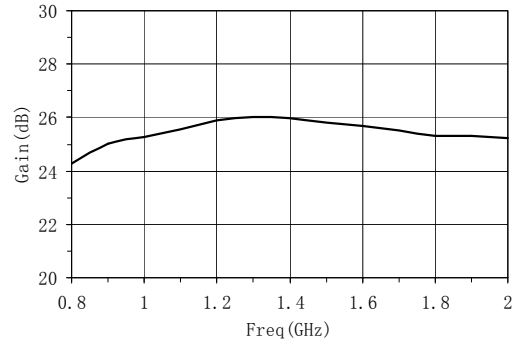
**Limited Rating Value**

VDS	+32V
VGS	-5V
Max Input CW Power	+25dBm
Channel Temperature	+175°C
Storage Temperature	-65°C~+150°C

**Typical Testing Curves**

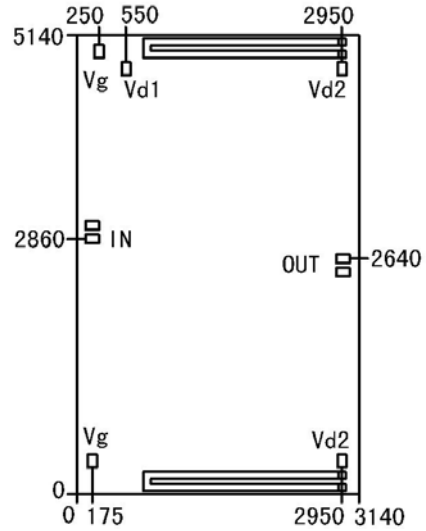


Power Gain vs. Frequency



**Dimension and Outline**

NC11611C-102P20 outlines



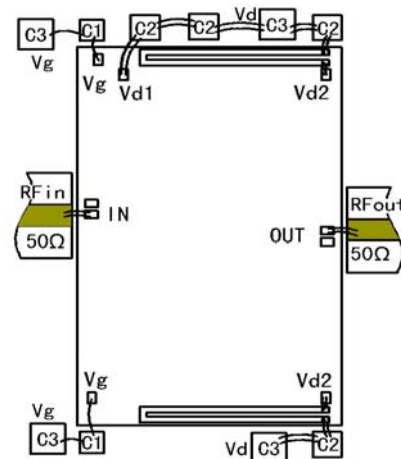
Note: The unit is μm.

Dimension of Input/Output pad: 150×100μm<sup>2</sup>.

Pad dimension of Vg: 100×150μm<sup>2</sup>.

Vd pad dimension: 100×150μm<sup>2</sup>.

**Assembly Diagram**



Note : External Capacitor C1=100pF, C2=1000pF, C3=10000pF.

**Attention**

1. Gold bonding wires of 25-30 $\mu$ m diameter are suggested to be used. The bonding platform temperature shall not exceed 250 $^{\circ}$ C.
  2. Blocking capacitors in Input/Output are already integrated.
  3. Bonding with 80/20 Au/Sn. Temperature should be lower than 300  $^{\circ}$ C and time should be less than 30 seconds.
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