

Features:

- Frequency: 2GHz~6GHz
- Power Gain: 25dB
- Psat: 43dBm
- P.A.E.: 30%
- +24V@2.2A(Quiescent)
- Chip size: 3.86mm×5.16mm×0.1mm

Electrical Specification (TA=+25°C, Vg=-2.2V, Vd=+24V)

| Parameter | Min. | Typ. | Max. | Unit |
|-------------------|---------|------|-------|------|
| Frequency | 2.0-6.0 | | | GHz |
| Psat | | 43.5 | | dBm |
| Power Gain | | 25 | | dB |
| Gain Flatness | | | ±0.75 | dB |
| P.A.E. | | 30 | | % |
| VSWRin | | | 2.8 | - |
| Operating Current | | | 4 | A |

Note: 1) All chips have been on-chip 100% DC and RF tested

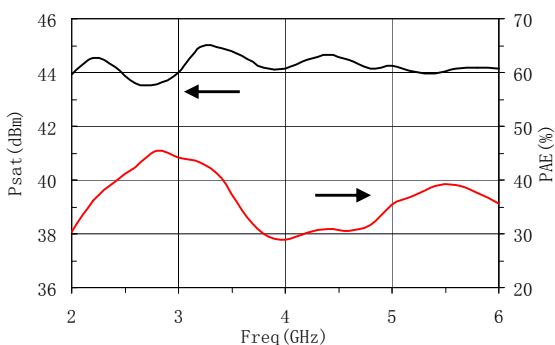
2) Test condition: Vd=+24V; Vg=-2.2V, pulse width 100µs, duty cycle 10%, P_m=18dBm

Limited Rating Values

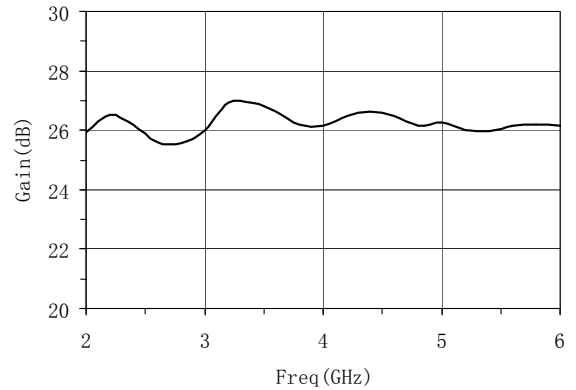
| | |
|---------------------|--------------|
| Vds | +32V |
| Vgs | -5V |
| Input CW Power | +25dBm |
| Channel Temperature | +175°C |
| Storage Temperature | -65°C~+150°C |

Typical Testing Curves

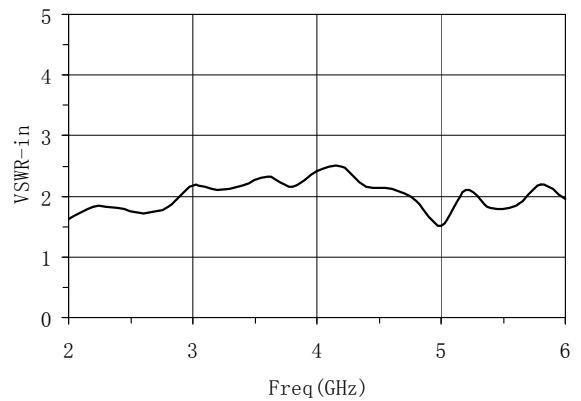
Output Psat/Efficiency VS Frequency



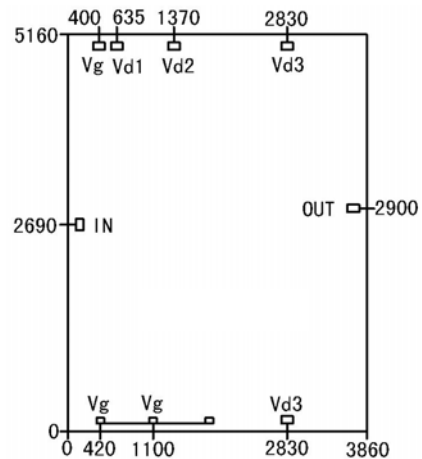
Power Gain VS Frequency



Input Voltage VSWR Ratio vs. Frequency



Dimensions and Outline



Note: All units in µm;

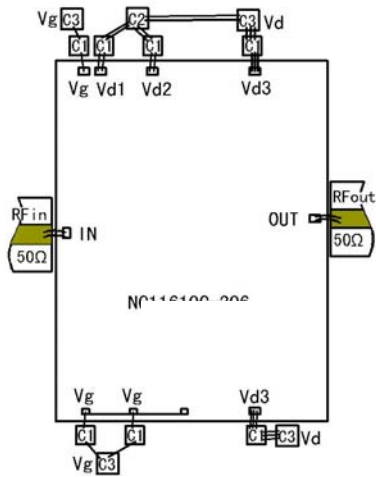
Dimension of Input Pad is 100×150µm².

Dimension of Output Pad is 150×100µm².

Dimension of Vd Pad is 150×100µm².

Dimension of Vg Pad is 100×80µm².

Assembly Diagram



Note: External capacitor C1=100pF,C2=1000pF,C3=10000pF.

Attention

- 1) Blocking capacitors in Input/Output are already integrated.
- 2) Bonding with Au:Sn=80%:20%. The temperature should be lower than 300°C and the time should be less than 30 seconds.
- 3) Gold wires of 25μm~30μm diameter should be used. Temperature of the bottom of bonding platform should be lower than 250°C.
- 4) Antistatic protection should be taken.