

**Features**

- Frequency: 13.5GHz~15.5GHz
- Power Gain: 20dB
- Psat: 45dBm
- P.A.E.: 30%
- +28V @ 2.5A (Quiescent)
- Chip Size: 4.0mm×3.7mm×0.1mm

**Electrical Specification (TA=+25°C, Vd=+28V, Vg=-2.5V)**

Parameter	Min.	Typ.	Max.	Unit
Frequency	13.5-15.5			GHz
Power Gain	19	20		dB
Psat	44.8	45.2		dBm
P.A.E.	30	33		%
VSWRin			2.5	-
Dynamic Operating Current	3.5			A

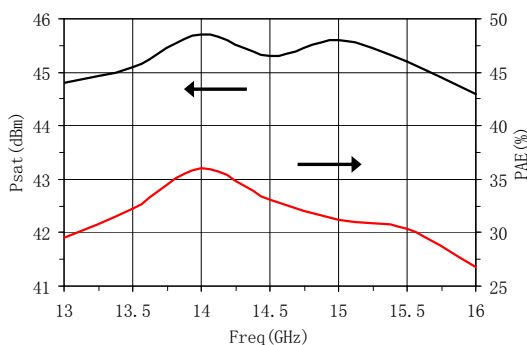
Note: 1) All chips have been on-chip 100% DC tested.  
 2) Test Condition: Vd=+28V, Vg=-2.5V, pulse width 100μs, duty cycle 10%, Pin=25dBm.

**Limited Rating Values**

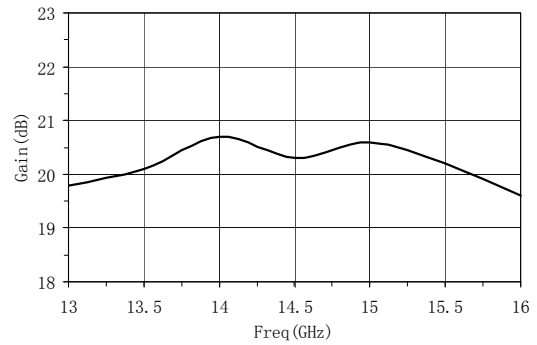
Max. Input Vd	+30V
Max. Input Power	+30dBm
Storage Temperature	-65°C ~ +150°C
Operating Temperature	-55°C ~ +85°C

**Typical Testing Curves**

Output Psat/Efficiency VS Frequency

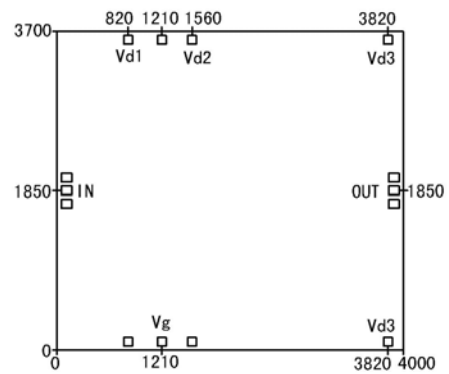


Power Gain VS Frequency



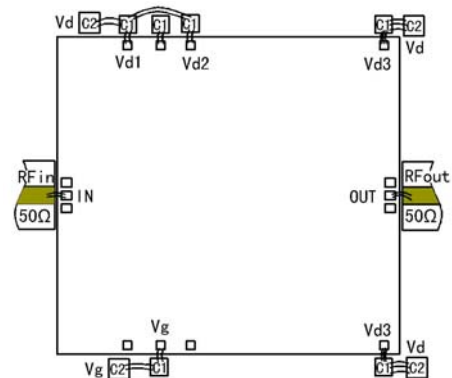
**Dimensions and Outline**

NC11602C-1315P30 outline



Note: The unit is μm. Dimension of input/output pad: 100×120μm<sup>2</sup>. Dimension of bias pad: 100×100μm<sup>2</sup>.

**Assembly Diagram**



Note: External capacitor c=100pF, c2=0.01μF. A 0.01μF capacitor should be added to gate bias. Diameter of gold wires: 25μm.

**Attention**

- 1) 2 bonding wires should be used for input/output. The length should be shorter than 350μm.
- 2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300°C and time should be less than 30 seconds.
- 3) Blocking capacitors in Input/Output are already integrated.
- 4) Antistatic protection should be taken.