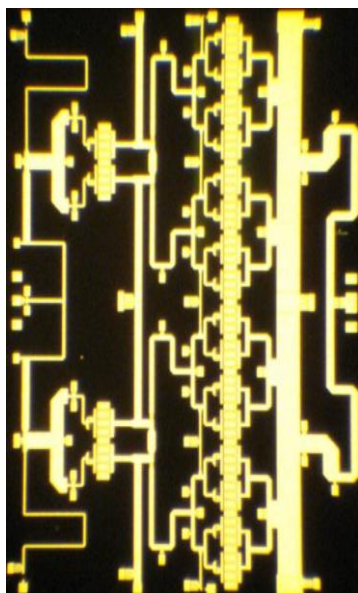


7.5-13.5 GHz GaAs MMIC Power Amplifier



Key Features

- X/K_u Band 10W Power Amplifier
- 15dB Large Signal Gain
- +40 dBm Saturated Output Power
- 35% power Added Efficiency

Applications

- Point-to-Point Radio
- Communications

Product Description

The SANDRA-SEMI SDC2018 is a two stage 7.5-13.5 GHz GaAs MMIC power amplifier has a large signal gain of 15 dB with a 40.0 dBm saturated output power. This MMIC uses 0.25um GaAs PHEMT device model technology, and is based upon optical gate lithography to ensure high repeatability and uniformity. The chip provides a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. The reliability of the chip has been verified through extensive tests.

Table1: RF Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|------------------------|------------------|------|---------|------|------|
| Frequency Range | Freq | 8 | | 13 | GHz |
| Input Return Loss | S11 | | -9 | | dB |
| Output Return Loss | S22 | | -10 | | dB |
| Large Signal Gain | S21 | | 15 | | dB |
| Saturated Output Power | P _{SAT} | | 40 | | dBm |
| Drain Bias Voltage | V _d | | 8 | | V |
| Gate Bias Voltage | V _g | -0.9 | -0.8 | -0.7 | V |

SDC2018

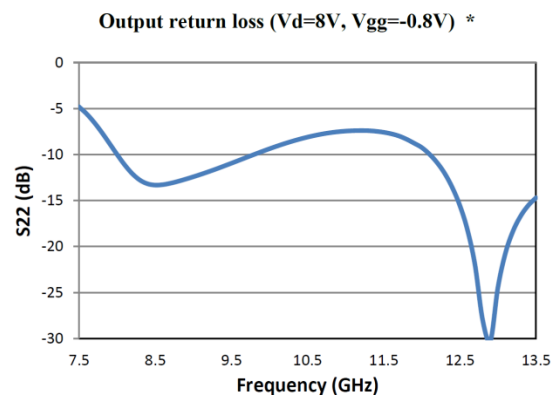
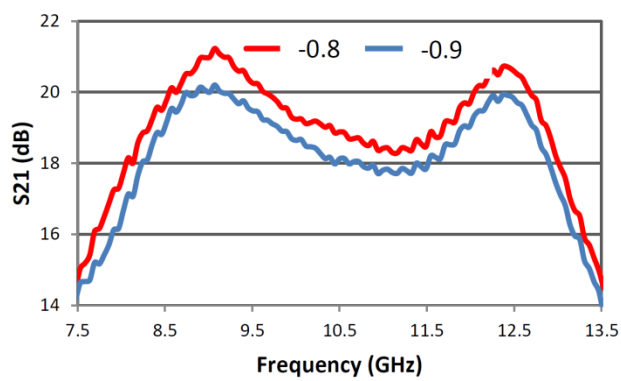
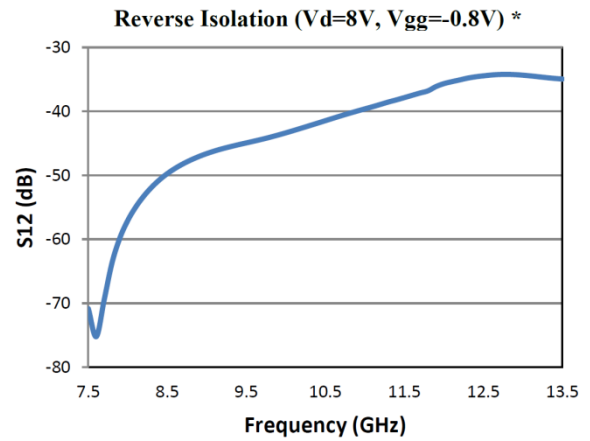
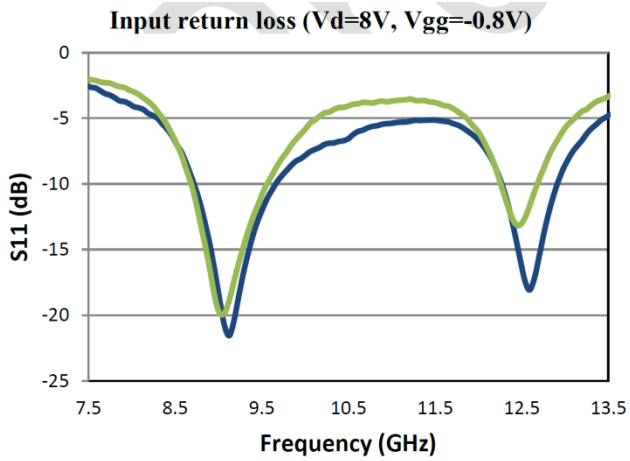
Absolute Maximum Ratings

| Parameter | Value |
|--------------------------|----------------|
| Drain Voltage | 8 |
| Gate Voltage 1, Vg1 | -0.8 |
| Gate Voltage 2, Vg2 | -0.8 |
| Drain Current, Id | 3.5 |
| Channel Temperature, Tch | 175 °C |
| Storage Temperature | -65 to +150 °C |

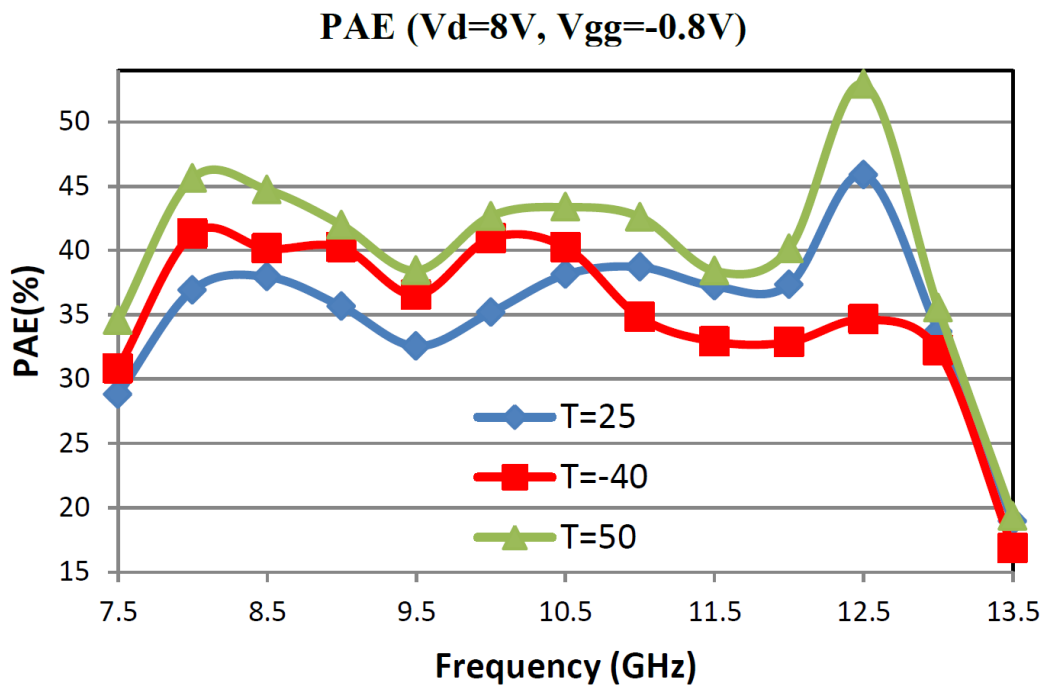
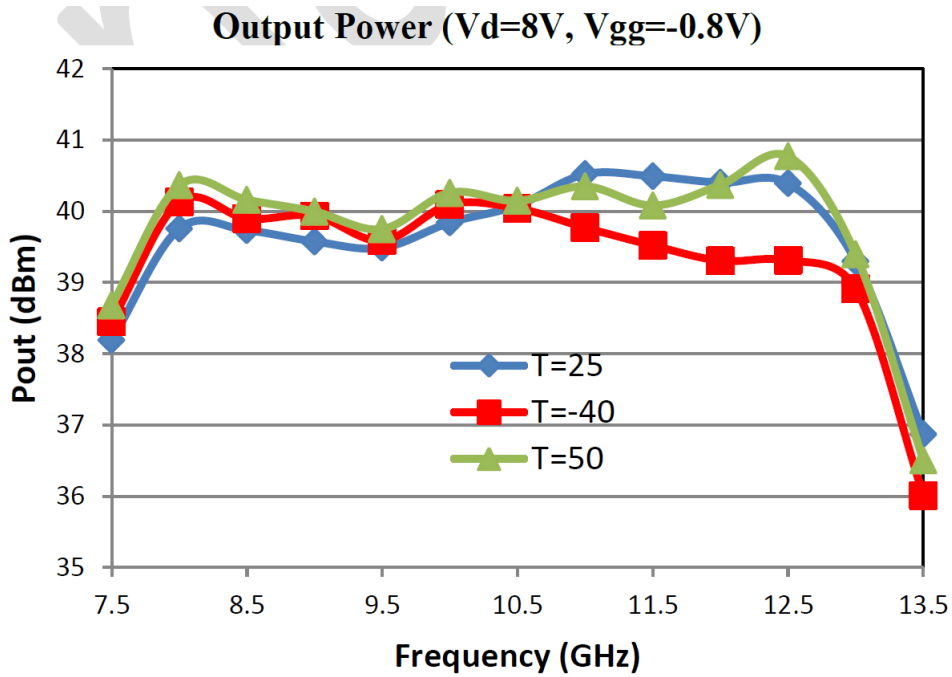
Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|-----------|------|------|-----|------|
| Vd | | 8 | | V |
| Id | | 3.5 | | A |
| Vg1 | | -0.8 | | V |
| Vg2 | -0.9 | -0.8 | 0.7 | V |

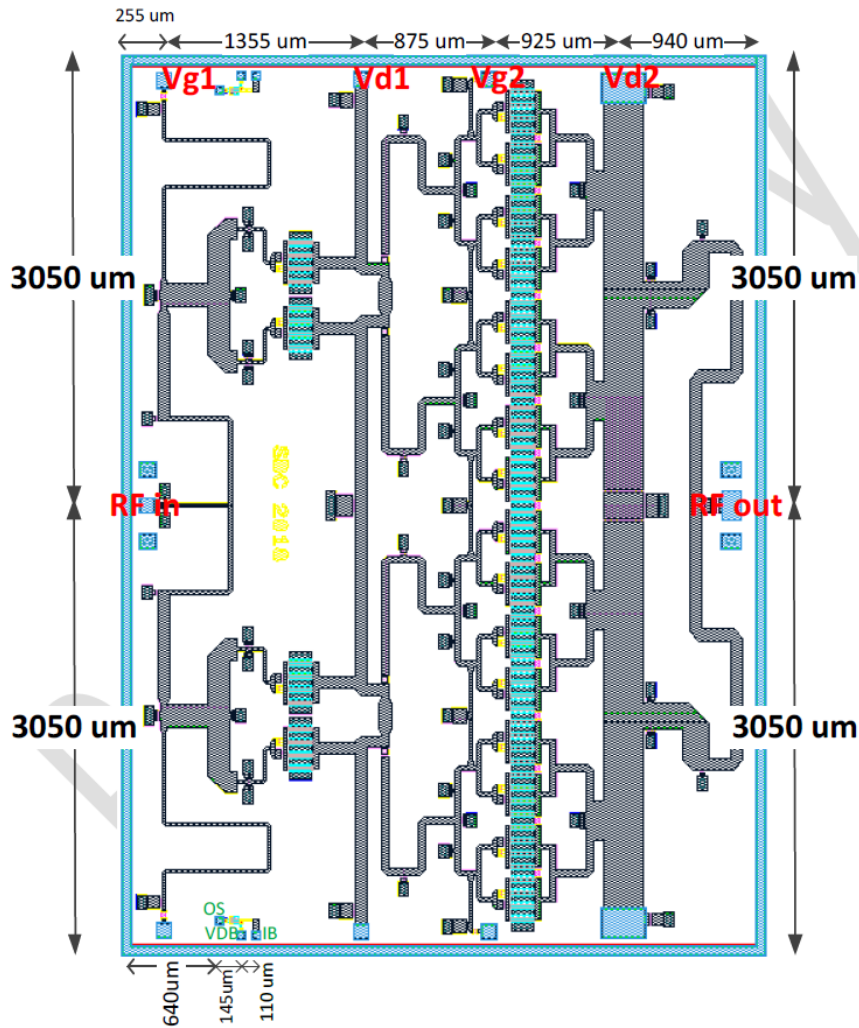
Small Signal Performance



Large Signal Performance



Mechanical Drawing



Pin Description

| Symbol | Description |
|-------------------|------------------------------------|
| Vg1 | Gate bias of first stage |
| Vd1 | Drain bias of first stage |
| Vg2 | Gate bias of second stage |
| Vd2 | Drain bias of second stage |
| RF _{in} | Input Signal |
| RF _{out} | Output Signal |
| VD | Drain bias of biasing circuit |
| OB | Control signal for biasing circuit |
| IB | Output of biasing circuit |